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| KONA_bk.png |
| Integration Guide / KONA2 Y2250N  **V1.0 (March. 2019)** |
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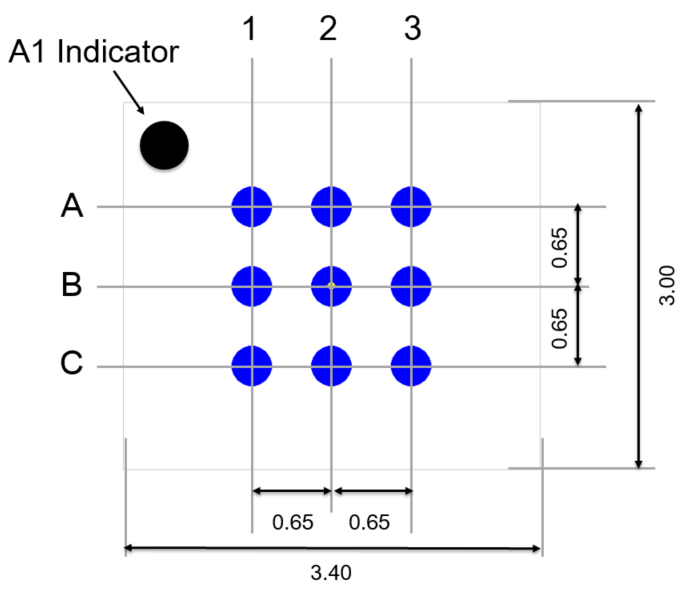
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1. Package Information

The KONA2 Y2250N supports only the 9FBGA package and other packages are not available.

* 1. 9FBGA Package Dimensions
  2. Brief Top View

(Unit: ㎜)

* 1. Chip Footprint

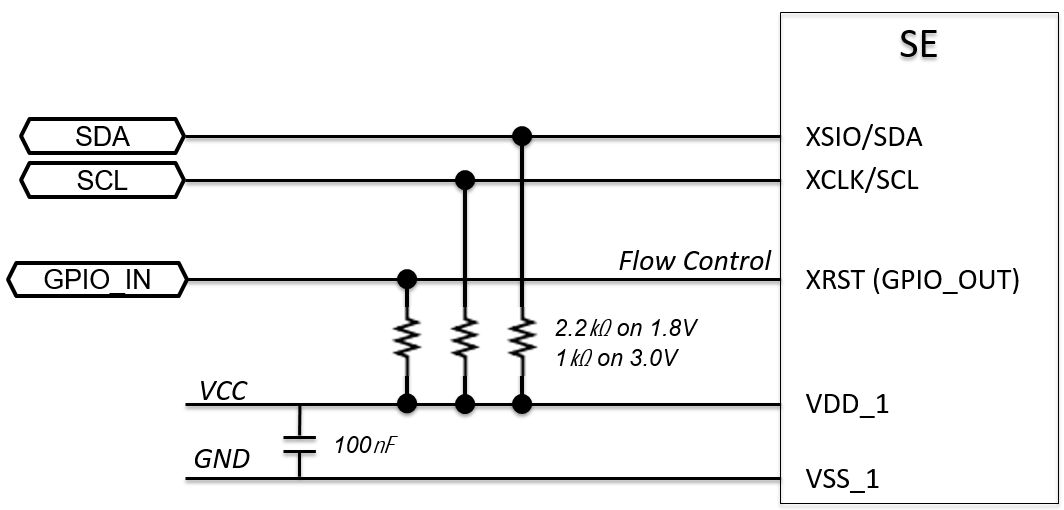
These footprint files are freely available.

|  |  |
| --- | --- |
| DXF | PCB |
|  |  |

* 1. Pin Map

|  |  |  |  |
| --- | --- | --- | --- |
|  | **1** | **2** | **3** |
| **A** | XCLK/SCL  (I2C\_CLK) | VSS\_1  (GND) | XSIO/SDA  (I2C\_DATA) |
| **B** | XRST  (Flow Control Pin) | VSS\_1  (GND) | VSS\_1  (GND) |
| **C** | VSS\_1  (GND) | VDD\_1  (VCC) | VSS\_1  (GND) |

1. Integration Guide



* 1. Pin Description
     1. VDD\_1

VDD\_1 can take three voltage levels: V1.8, V3.0, and V5.0

* + 1. VSS\_1

VSS\_1 shall be connected to the GND.

* + 1. XSIO/SDA and XCLK/SCL

XSIO/SDA and XCLK/SCL are used for I2C communication and these lines shall be connected to a pull-up register.

* + 1. XRST

XRST has two modes of ‘RESET’ and ‘Flow Control’.

* RESET: During power-on time, XRST shall have high level.
* Flow Control: After power-on time, it acts as a GPIO\_OUT indicating the SE busy state.

**Caution!**

**- I2C Host does not need to handle the flow control, it is handled by the SE Library.**

* 1. I2C Information
* Slave Address: 0x23
* Speed: Normal
  1. Basic Test

|  |  |  |  |
| --- | --- | --- | --- |
| Step | I2C W/R | Data / Length | Description |
| 1 | Write | 02 00 00 00 10 | Generate Random |
| 2 | Read | 2 bytes | Length of SE Response |
| 3 | Read | 18 bytes | Random Values |

1. Electrical Data
   1. General DC Electrical Characteristics

* Temperature -25℃ ~ +85℃, VDD 1.62V ~ 5.5V

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Conditions | Min. | Typ. | Max. | Unit |
| Input low voltage  (VIL) | SIO | -0.3 | - | 0.2 VDD | V |
| Clock | -0.3 | - | 0.2 VDD |
| Reset | -0.3 | - | 0.2 VDD |
| Input low current  (IIL) | SIO | -500 | - | + 20 | ㎂ |
| Clock | -20 | - | + 20 |
| Reset | -50 | - | + 20 |
| Input high voltage  (VIH) | SIO | 0.7 VDD | - | VDD + 0.3 | V |
| Clock | 0.7 VDD | - | VDD + 0.3 |
| Reset | 0.7 VDD | - | VDD + 0.3 |
| Input high current  (IIH) | SIO | -300 | - | + 20 | ㎂ |
| Clock | -20 | - | + 20 |
| Reset | -20 | - | + 20 |
| Output low voltage  (VOL) | IOL = 1000㎂, SIO,  VDD = 4.5 V | 0  (NOTE) | - | 0.08 VDD | V |
| IOL = 1000㎂, SIO,  VDD = 2.7 V | 0  (NOTE) | - | 0.4 |
| IOL = 1000㎂, SIO,  VDD = 1.62 V | 0  (NOTE) | - | 0.3 |
| IOL = 500㎂, SIO,  VDD = 1.62 V | 0  (NOTE) | - | 0.15 VDD |
| Output high voltage  (VOH) | IOH = -20㎂, SIO | 0.7 VDD | - | VDD |  |

NOTE: To allow for overshoot the voltage on IO, CLK and RESET shall remain between -0.3V and Vcc +0.3V during dynamic operations.

* 1. Absolute Maximum Rating

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Conditions | Rating. | Unit |
| Supply voltage (VDD) | TA = 25℃ | – 0.3 to + 7.0 | V |
| Input voltage (VIN) | TA = 25℃ | – 0.3 to VDD + 0.3 |
| Output voltage (VO) | TA = 25℃ | – 0.3 to VDD + 0.3 |
| Operating temperature (TA) | - | – 25 to + 85 | ℃ |
| Storage temperature | - | – 65 to + 150 |
| Electrostatic discharge | TA = 25℃ | 4000 | V |